WHAT IS CLAIMED IS:

1. A method of measuring an injection lock frequency range for an integrated circuit having a first voltage-controlled oscillator and a second voltage-controlled oscillator, the method comprising the steps of:

applying a control voltage to an input of the second voltage-controlled oscillator such that an output frequency of the second voltage-controlled oscillator locks to an output frequency of the first voltage-controlled oscillator; and

varying the output frequency of the first voltage-controlled oscillator until the output frequency of the second voltage-controlled oscillator falls out of lock with the output frequency of the first voltage-controlled oscillator.

2. A method as in claim 1,

wherein the step of applying the control voltage to the input of the second voltage-controlled oscillator involves the step of switching the input of the second voltage-controlled oscillator from an output of a low pass filter to a control signal to which the control voltage is applied.

3. A method as in claim 2, wherein the step of applying the control voltage to the input of the second voltage-controlled oscillator further involves the step of:

monotonically changing the control voltage until the output frequency of the second voltage-controlled oscillator locks to the output frequency of the first voltage-controlled oscillator.

4. A method as in claim 1,

wherein the first voltage-controlled oscillator is an element of a first phase-locked loop.

5. A method as in claim 4, wherein the step of varying the output frequency of the first voltage-controlled oscillator involves the step of:

changing a frequency of an input stream to the first phase-locked loop.

6. A method as in claim 5,

wherein the second voltage-controlled oscillator is an element of a second phase-locked loop.

7. A method of computing an injection signal power within a voltage-controlled oscillator on an integrated circuit, the method comprising the steps of:

determining an injection lock frequency range of the voltage-controlled oscillator;

determining a que of an LC tank within a voltage-controlled oscillator;

determining a free-run frequency of the voltage-controlled oscillator;

determining a free-run output power of the voltage-controlled oscillator; and

calculating an injection signal power value proportional to a product of a square of the injection lock frequency range, a square of the que, and the free-run output power of the voltage-controlled oscillator divided by a square of the free-run output frequency of the voltage-controlled oscillator.

8. A method as in claim 7, wherein the step of determining an injection lock frequency range comprises the step of measuring an injection lock frequency range of the voltage-controlled oscillator.

9. A method as in claim 8, wherein the step of measuring the injection lock frequency range of the voltage-controlled oscillator comprises the steps of:

applying a control voltage to an input of the voltage-controlled oscillator such that the output frequency of the voltage-controlled oscillator locks to an output frequency of another voltage-controlled oscillator on the integrated circuit; and

varying the output frequency of the voltage-controlled oscillator until the output frequency of the voltage-controlled oscillator falls out of lock with the other voltage-controlled oscillator.

10. A method as in claim 9, further comprising the steps of:

wherein the step of applying the control voltage to the input of the voltage-controlled oscillator involves the step of switching the input of the voltage-controlled oscillator from an output of a low pass filter to a control signal to which the control voltage is applied.

11. A method as in claim 10, wherein the step of applying the control voltage to the input of the second voltage-controlled oscillator further involves the step of:

monotonically changing the control voltage until the output frequency of the second voltage-controlled oscillator locks to the output frequency of the first voltage-controlled oscillator.

12. A method as in claim 7,

wherein the other voltage-controlled oscillator is an element of a first phase-locked loop.

13. A method as in claim 12, wherein the step of varying the output frequency of the other voltage-controlled oscillator comprises the step of:

changing a frequency of an input stream to the first phase-locked loop.

14. A method as in claim 13,

wherein the voltage-controlled oscillator is an element of a second phase-locked loop.

15. A method of reducing an injection lock frequency range of a second voltage-controlled oscillator in an integrated circuit having first and second voltage-controlled oscillators, the method comprising the steps of:

measuring an injection lock frequency range of the second voltage-controlled oscillator; and

increasing a free-run output power of the second voltage-controlled oscillator.

16. A method as in claim 15, wherein the step of measuring the injection lock frequency range of the second voltage-controlled oscillator comprises the steps of:

applying a control voltage to an input of the second voltage-controlled oscillator such that an output frequency of the second voltage-controlled oscillator locks to an output frequency of the first voltage-controlled oscillator; and

varying the output frequency of the first voltage-controlled oscillator until the output frequency of the second voltage-controlled oscillator falls out of lock with the output frequency of the first voltage-controlled oscillator.

17. A method as in claim 16,

wherein the step of applying the control voltage to the input of the second voltage-controlled oscillator involves the step of switching the input of the second voltage-controlled oscillator from an output of a low pass filter to a control signal to which the control voltage is applied.

18. A method as in claim 17, wherein the step of applying the control voltage to the input of the second voltage-controlled oscillator further involves the step of:

monotonically changing the control voltage until the output frequency of the second voltage-controlled oscillator locks to the output frequency of the first voltage-controlled oscillator.

19. A method as in claim 16, wherein the first voltage-controlled oscillator is an element of a first phase-locked loop.

20. A method as in claim 19, wherein the step of varying the output frequency of the first voltage-controlled oscillator involves the step of:

changing a frequency of an input stream to the first phase-locked loop.

21. A method as in claim 20, wherein the second voltage-controlled oscillator is an element of a second phase-locked loop.

22. A method as in claim 15, wherein the step of increasing the free-run output power of the second voltage-controlled oscillator is accomplished by increasing a signal amplitude of the second voltage-controlled oscillator.

23. A method as in claim 15, wherein the step of increasing the free-run output power of the second voltage-controlled oscillator is accomplished by reducing a loading of an output signal of the second voltage-controlled oscillator.

24. A method as in claim 19, further comprising the step of:

increasing a loop bandwidth in the first phase-locked loop.

25. A method as in claim 24, wherein the step of increasing the loop bandwidth in the first phase-locked loop is accomplished by increasing a pass band of a loop filter within the first phase-locked loop.

26. A method of reducing intermodulation between a first voltage-controlled oscillator (VCO) in a first phase-locked loop (PLL) and a second VCO in a second PLL, comprising:

measuring an injection lock frequency range of the second VCO with respect to the first VCO;

measuring a signal power of the second VCO;

determining a crosstalk power between the first and the second VCOs using the measured injection lock frequency range and the measured signal power of the second VCO; and

adjusting a signal power ratio between the first VCO and the second VCO to reduce intermodulation.

27. The method of claim 26 further comprising adjusting a loop bandwidth of the first PLL relative to that of the second PLL to reduce intermodulation.

28. The method of claim 27 wherein the first PLL is part of a transmitter and the second PLL is part of a receiver, and wherein the step of adjusting a signal power ration comprises increasing a power of the first VCO relative to that of the second VCO.

29. The method of claim 28 wherein the step of adjusting a loop bandwidth comprises increasing a loop bandwidth of the second PLL relative to that of the first PLL.

30. A transceiver circuit comprising:

a transmitter having a first phase-locked loop (PLL), the first PLL having a first voltage-controlled oscillator (VCO);

a receiver having a second PLL, the second PLL having a second VCO; and

a parasitic loop that couples signals between the transmitter and the receiver causing intermodulation,

wherein, the first VCO is configured to have a different power level relative to that of the second VCO to reduce the intermodulation.

31. The transceiver of claim 30 wherein the first VCO is configured to have a power level that is greater than that of the second VCO.

32. The transceiver of claim 30 wherein the first PLL is configured to have a bandwidth that is different than a bandwidth of the second PLL.

33. The transceiver of claim 32 wherein the second PLL is configured to have a bandwidth that is greater than the bandwidth of the first PLL.

34. The transceiver of claim 31 wherein the second PLL is configured to have a bandwidth that is greater than a bandwidth of the first PLL.